

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating a transistor, said method comprising:

forming a gate stack over a semiconductor substrate, said gate stack comprising a gate oxide layer, a conducting layer, and a first insulating layer;

forming first sidewall spacers on the sides of said gate stack;

forming source and drain regions on opposite sides of said gate stack;

forming a second insulating layer over said gate stack and substrate;

removing at least a portion of said second insulating layer and said first insulating layer of said gate stack to expose said conducting layer; and,

forming at least one silicide layer over and in contact with said exposed conducting layer.

2. A method as in claim 1, wherein said conducting layer comprises a polysilicon layer said method further comprising forming said silicide layer by providing at least one metal containing layer over said polysilicon layer and processing said metal containing layer and polysilicon to form said silicide layer.

3. A method as in claim 1, wherein said first insulating layer is silicon nitride.

4. A method as in claim 1, further comprising forming source/drain implants in said substrate which are self-aligned to said gate stack before forming said first sidewall spacers.
5. A method as in claim 4, wherein said implants are angled implants.
6. A method as in claim 5, wherein said implants are LDD implants.
7. A method as in claim 4, wherein said first sidewall spacers are formed by a spacer-forming insulating layer over said gate stack and substrate and etching said spacer-forming layer to produce said first sidewall spacers.
8. A method as in claim 7, wherein said spacer-forming layer is an oxide layer.
9. A method as in claim 1, wherein said source and drain regions are formed after said first sidewall spacers are formed.
10. A method as in claim 9, wherein lightly doped regions are formed in said substrate on opposite sides of said gate stack before said first sidewall spacers are formed.
11. A method as in claim 1, wherein said second insulating layer is a nitride layer.

12. A method as in claim 1, further comprising forming at least one channel implant region in said substrate through said gate stack after said conducting layer is exposed and before said silicide layer is formed.
13. A method as in claim 12, wherein said at least one channel implant region is at least in part defined by said first sidewall spacers.
14. A method as in claim 11, further comprising, prior to forming said silicide layer, forming second sidewall spacers over and at sides of said exposed conductor layer and forming a channel implant region through said gate stack wherein said channel implant region is at least in part defined by said second sidewall spacers.
15. A method as in claim 1, wherein a portion of said second insulating layer outside of said first sidewall spacers remains after said at least a portion of said insulating layer is removed, said method further comprising, prior to forming said silicide layer, removing another portion of said second insulating layer adjacent to said first sidewall spacers and an upper portion of said first sidewall spacers; and forming a channel implant region through said gate stack in said substrate which is at least in part defined by removed portions of said second insulating layer.
16. A method as in claim 14, wherein said first channel implant region is formed to be narrower in width than the gate stack.

17. A method as in claim 13, wherein said channel implant region is formed to be approximately equal in width to the gate stack.
18. A method as in claim 15, wherein said channel implant region is formed to be wider in width than the gate stack.
19. A method as in claim 13, further comprising, prior to forming said silicide layer, forming second sidewall spacers over and at sides of said exposed conductor layer and forming another channel implant region through said gate stack wherein said another channel implant region is at least in part defined by said second sidewall spacers.
20. A method as in claim 13, wherein a portion of said second insulating layer outside of said first sidewall spacers remains after said at least a portion of said insulating layer is removed, said method further comprising, prior to forming said silicide layer, removing another portion of said second insulating layer adjacent to said first sidewall spacers and an upper portion of said first sidewall spacers; and forming another channel implant region through said gate stack in said substrate which is at least in part defined by removed portions of said second insulating layer.
21. A method as in claim 2, wherein said metal containing layer contains a material selected from the group consisting of tungsten(W), WSi_x, WN, Ti, TiN, and other combinations thereof.

22. A transistor structure comprising:

- a semiconductor substrate;
- a gate stack provided over said substrate, said gate stack comprising:
 - a gate oxide layer provided on said substrate;
 - a polysilicon layer provided on said gate oxide layer;
 - at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,
 - source and drain regions provided in said substrate on opposite sides of said gate stack.

23. A structure as in claim 22, further comprising first sidewall spacers on sidewalls of said gate stack.

24. A structure as in claim 23, further comprising second sidewall spacers provided over and at edges of said conducting layer.

25. A structure as in claim 23, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers.

26. A structure as in claim 24, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.
27. A structure as in claim 23, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.
28. A structure as in claim 27, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
29. A structure as in claim 25, further comprising second sidewall spacers provided over and at edges of said conducting layer.
30. A structure as in claim 29, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.
31. A structure as in claim 25, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

32. A structure as in claim 31, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
33. A structure as in claim 22, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.
34. A system comprising:
- a processor; and
 - a memory device coupled to said processor, at least one of said processor and said memory device comprising a transistor structure, said transistor structure comprising:
 - a semiconductor substrate;
 - a gate stack provided over said substrate, said gate stack comprising:
 - a gate oxide layer provided on said substrate;
 - a polysilicon layer provided on said gate oxide layer;
 - at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

35. A structure as in claim 34, further comprising first sidewall spacers on sidewalls of said gate stack.

36. A system as in claim 35, further comprising second sidewall spacers provided over and at edges of said conducting layer.

37. A system as in claim 35, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers.

38. A system as in claim 36, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

39. A system as in claim 35, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

40. A system as in claim 39, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
41. A system as in claim 37, further comprising second sidewall spacers provided over and at edges of said conducting layer.
42. A system as in claim 41, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.
43. A system as in claim 37, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.
44. A system as in claim 43, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
45. A system as in claim 34, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x , WN, Ti, TiN, and combinations thereof.
46. A method of fabricating a transistor, said method comprising:

forming a gate stack over a semiconductor substrate, said gate stack comprising a gate oxide layer, a conducting layer, and a first insulating layer;
forming first sidewall spacers on the sides of said gate stack;
forming source and drain regions on opposite sides of said gate stack;
forming a second insulating layer over said gate stack and substrate;
removing at least a portion of said second insulating layer and said first insulating layer of said gate stack to expose said conducting layer;
forming at least one additional set of second spacers over and at sides of said exposed conducting layer;
forming a plurality of channel implant regions in said substrate through said gate stack after said conducting layer is exposed, wherein said plurality of channel implant regions are at least in part defined by said first sidewall spacers and said at least one additional set of second spacers; and,
forming at least one silicide layer over and in contact with said exposed conducting layer.

47. A method as in claim 46, wherein said conducting layer comprises a polysilicon layer said method further comprising forming said silicide layer by providing at least one unetched metal-containing layer over said polysilicon layer and processing said unetched metal-containing layer and polysilicon to form said silicide layer.

48. A method as in claim 46, wherein said first insulating layer is silicon nitride.

49. A method as in claim 46, further comprising forming source/drain implants in said substrate which are self-aligned to said gate stack before forming said first sidewall spacers.
50. A method as in claim 49, wherein said implants are angled implants.
51. A method as in claim 50, wherein said implants are LDD implants.
52. A method as in claim 49, further comprising forming a spacer-forming insulating layer over said gate stack and substrate and etching said spacer-forming layer to produce said first sidewall spacers.
53. A method as in claim 52, wherein said spacer-forming layer is an oxide layer.
54. A method as in claim 46, wherein said source and drain regions are formed after said first sidewall spacers are formed.
55. A method as in claim 54, wherein lightly doped regions are formed in said substrate on opposite sides of said gate stack before said spacers are formed.
56. A method as in claim 46, wherein said second insulating layer is a nitride layer.

57. A method as in claim 46, further comprising forming a plurality of channel implant regions in said substrate through said gate stack after said conducting layer is exposed and before said silicide layer is formed.
58. A method as in claim 46, wherein a portion of said second insulating layer outside of said first sidewall spacers remains after said at least a portion of said insulating layer is removed, said method further comprising, prior to forming said silicide layer, removing another portion of said second insulating layer adjacent to said first sidewall spacers and an upper portion of said first sidewall spacers; and forming at least one channel implant region through said gate stack in said substrate which is at least in part defined by removed portions of said second insulating layer.
59. A method as in claim 46, wherein said channel implant regions are formed to be narrower in width than the gate stack.
60. A method as in claim 46, wherein said channel implant regions are formed to be approximately equal in width to the gate stack.
61. A method as in claim 58, wherein said channel implant region is formed to be wider in width than the gate stack.
62. A method as in claim 46, wherein a portion of said second insulating layer outside of said first sidewall spacers remains after said at least a portion of said

insulating layer is removed, said method further comprising, prior to forming said silicide layer, removing another portion of said second insulating layer adjacent to said first sidewall spacers and an upper portion of said first sidewall spacers; and forming at least another channel implant region through said gate stack in said substrate which is at least in part defined by removed portions of said second insulating layer.

63. A method as in claim 47, wherein said metal containing layer contains a material selected from the group consisting of W, WSi_x , WN, Ti, TiN, and other combinations thereof.

64. A gate stack structure provided on a semiconductor substrate comprising:

- a gate oxide layer provided on said substrate;
- a conducting layer provided on said gate oxide layer;
- first sidewall spacers on sidewalls of said gate stack;
- at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers;
- second sidewall spacers provided over and at edges of said conducting layer;
- at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers
- at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

65. A structure as in claim 64, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.
66. A structure as in claim 65, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
67. A structure as in claim 64, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.
68. A structure as in claim 67, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.
69. A structure as in claim 64, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

70. A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

at least one channel implant region in said substrate below said gate stack,

which is defined at least in part by said first sidewall spacers;

at least one unetched silicide layer formed over and in contact with said
conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said
gate stack.

71. A structure as in claim 70, wherein said conducting layer is polysilicon.

72. A structure as in claim 70, further comprising an insulating layer adjacent to said
first sidewall spacers, said insulating layer and said first sidewall spacers having
etched out upper portions to define an area extending beyond a lateral width of
said gate stack.

73. A structure as in claim 72, further comprising at least one channel implant
region in said substrate below said gate stack, which is defined at least in part by
said area.

74. A structure as in claim 70, wherein said silicide layer is formed of a material in the group consisting of W, WSi₂, WN, Ti, TiN, and other combinations thereof.

75. A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

second sidewall spacers provided over and at edges of said conducting layer;

at least one channel implant region in said substrate below said gate stack,

which is defined at least in part by said second sidewall spacers;

at least one unetched silicide layer formed over and in contact with said

conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

76. A structure as in claim 75, wherein said conducting layer is polysilicon.

77. A structure as in claim 75, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having

etched out upper portions to define an area extending beyond a lateral width of said gate stack.

78. A structure as in claim 77, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

79. A structure as in claim 77, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

80. A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

an insulating layer adjacent to said first sidewall spacers, said insulating layer

and said sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack;

at least one channel implant region in said substrate below said gate stack,

which is defined at least in part by said area;

at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

81. A structure as in claim 80, wherein said conducting layer is polysilicon.
82. A structure as in claim 80, further comprising second sidewall spacers provided over and at edges of said conducting layer.
83. A structure as in claim 82, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.
84. A structure as in claim 80, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x , WN, Ti, TiN, and other combinations thereof.
85. A transistor structure comprising:
- a semiconductor substrate;
 - a gate stack provided over said substrate, said gate stack comprising:
 - a gate oxide layer provided on said substrate;
 - a conducting layer provided on said gate oxide layer;
 - first sidewall spacers provided on sidewalls of said gate stack;

an insulating layer adjacent to said first sidewall spacers, said insulating layer and said sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack;
second sidewall spacers provided over and at edges of said conducting layer;
at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers;
at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,
source and drain regions provided in said substrate on opposite sides of said gate stack.

86. A structure as in claim 85, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x , WN, Ti, TiN, and combinations thereof.
87. A method of fabricating a gate structure of a transistor, said method comprising:
forming an oxide layer over a substrate;
forming a conducting layer over said oxide layer;
forming an insulating layer over said conducting layer;
removing portions of said oxide layer, said conducting layer, and said insulating layer to form a gate stack, said gate stack having an oxide layer, a conducting layer, and an insulating layer;
removing said insulating layer from said gate stack to expose said conducting layer; and,

providing a metal-containing layer on said exposed conducting layer which can form a silicide.

88. A method as in claim 87, wherein said conducting layer comprises a polysilicon layer.

89. A method as in claim 87, wherein said step of forming said silicide further comprises providing at least one unetched metal-containing layer over said exposed conducting layer and processing said unetched metal-containing layer and conducting layer to form said silicide layer.

90. A method as in claim 87, wherein said metal-containing layer is an unetched metal layer.

91. A method as in claim 90, wherein said unetched metal layer contains a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.